AMENDMENTS TO THE DRAWINGS:

Fig. 1 of the drawings was amended to include the reference character 28c, which is discussed with regard to the description of the drawings.

Attachments:

An Appendix including a replacement sheet for Fig. 1 of the drawings.

REMARKS:

Reconsideration and allowance of the above-identified application, as currently amended, is respectfully requested. The title of the invention was amended to conform to subject matter covered by the pending claims, in keeping with the outstanding requirement directed thereto. Acceptance of the amended title is respectfully requested.

Several editorial revisions were implemented in the Specification to remove a discovered informality as well as enhance the clarity therein. These revisions involve a spelling correction of the term silicon, and a revision of the expression "wiring 25" to that of "wiring 25a, 25b" so as to appropriately conform to the related reference characters in the drawings. The third revision effected more clearly describes the "silicon tower 24" in Fig. 1 of the drawings, etc., in terms of its related parts, namely, the impurity diffusion regions 28a and 28b and the channel region 28c which is sandwiched between them and in which parts 28a, 28c and 28b form the source-to-drain region of vertical transistor 21. This channel region 28c which is discussed on page 10, the second full paragraph thereof, on page 16, line 2 thereof, etc., of the original specification, is being appropriately labeled in Fig. 1 of the drawings for the purpose of conforming with the USPTO requirements pertaining thereto. Acceptance of the attached replacement sheet directed to Fig. 1 of the drawings is therefore respectfully requested.

Applicants note with appreciation the indication that claims 3, 6, 7 and 9 are directed to allowable subject matter and that these claims would be formally allowed upon being re-presented in an appropriate self-contained format. Accordingly, each of these claims was amended to incorporate the contents of the corresponding independent claim as well as any intervening claim thereof. In this regard, the now

amended independent claim 3 is inclusive of the contents of base claim 1 thereof. Likewise, each of claims 6, 7 and 9 was re-presented as an independent claim, respectively incorporating the subject matter of base claim 2 thereof. Correspondingly, Claims 1 and 2 were canceled. Any and all revisions implemented to the language previously existing is strictly to enhance the clarity thereof as well as avoid any previously raised matters such as that detailed in the outstanding objection to the drawings and in the rejection under 35 U.S.C. 112, second paragraph.

Regarding the expression "a layering direction", previously existing in claims 1 and 2, the contents of which are now contained in amended claims 3 and 6 – 9, the objection thereof was rendered moot in view of the clarifying revision made thereto. As can be seen from Fig. 1 of the drawings, for example, the channel region 28c of the gate pillar 24 is positioned between impurity regions 28a and 28b in a vertically extending direction with respect to a principal side of the semiconductor substrate, which should be clearly understood by one of ordinary skill. This is consistent with the related description of the tower-like gate pillar 24 in the Specification, noted also in the above discussion in these remarks. Regarding the expression "a gate electrode film formed so as to enclose an outer circumferential side of said gate pillar," it has been revised so that this expression now reads as "gate electrode is formed on said gate insulation film so as to enclose an outer circumferential side of said gate pillar," consistent with that shown in the drawings. Regarding the expression "so as to enclose an outer circumferential side of said gate pillar," an example support thereof is found on page 4, second paragraph, and on page 26, first paragraph thereof, of the Specification. With regard to the illustrated example embodiments, the multi-layered gate electrode film which encloses the outer circumferential side of the gate pillar, is formed on a gate insulation film (e.g., 23).

In view of the above-made clarifying revisions and related discussion, reconsideration/withdrawal of the objection to the drawings as well as the rejection under 35 U.S.C. 112, second paragraph, is respectfully requested.

An art rejection was given, also, under 35 U.S.C. 102(b), as specified in Item 8, in the Detailed Action. It is submitted, however, this rejection to claims 1 and 2 was rendered moot in view of the canceling of those claims. Moreover, insofar as this rejection is applicable to claim 8, it has been overcome in view of the amendments made thereto, as described below.

Regarding claim 8, it has been re-presented as an independent claim, incorporating the contents of base claim 2 (now canceled). The subject matter previously existing in original dependent claim 8 was modified so that the set forth "second electrode film" of the gate electrode is made of material such as that discussed by the example showings in the paragraph bridging pages 17 and 18 of the Specification. In this regard, at least for the reason that the set forth "second electrode film" is a metal silicide compound, the invention according to the now amended claim 8, it is submitted, is considered patentable over the teachings of Sung (U.S. Patent 6,198,121). That is, Sung neither disclosed nor suggested a semiconductor device having the set forth featured aspects as that now defined in claim 8. Structuring a gate electrode film to include a polycrystalline silicon film to enclose the gate pillar circumferentially and, also, a second electrode film which includes one of the metal silicide films mentioned in the paragraph bridging pages 17 – 18 of the original Specification, leads to, among other advantages, a reduction in the electrically resistance of the gate electrode and, in comparison to the case of using tungsten such as disclosed by Sung, a reduction in stress that occurs between the first electrode made of polycrystalline silicon and the second electrode film.

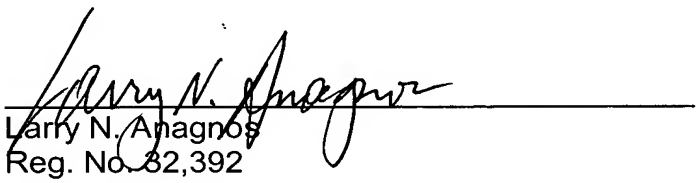
Accordingly, for at least the above reasons, claim 8, as currently amended, should also be rendered allowable.

Applicants submit, agreeing to the canceling of rejected claims as well as to the above-discussed modification to claim 8 should not be construed as acquiescence of the previously standing art rejection. In other words, the canceling of the claims as well as modification effected thereto were made without prejudice or disclaimer of the subject matter as previously existed.

Therefore, in view of the above-made amendments together with these accompanying remarks, favorable action on the currently pending claims, i.e., claims 3, 6 – 9, and an early formal notification of allowance of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (520.43863X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



Larry N. Anagnos
Reg. No. 32,392

LNA/gjb
(703) 312-6600